APPLICATION NOTE

HiBlade 48V Solid-State Battery

Multi-Tier Protection Architecture and
Automatic Pre-Charge Management

Architecture: 14S3P, 135Ah, 50.0 V nom.
BMS platform: Safiery Quasar + NXP BJB
Compliance: UL and DNV marine ready
Date: October 2026

5,000 A	80 A / < 350 A	400 A (100 µs)	UL/DNV Ready
Prospective inrush managed	Active ramp / peak at handover	Resettable solid-state SCP	NXP BJB pyro-fuse backup

1. Executive Overview: Solid-State Longevity Meets High-Power Inverters

Modern 48V marine, defence, and off-grid power systems pair ultra-low-impedance lithium battery banks with large multi-kilowatt inverter-chargers (such as single or parallel Victron MultiPlus and Quattro arrays). When energised from 0 V, an inverter's internal DC-link capacitor bank (10,000 µF to 40,000 µF) behaves like a dead short circuit for the first 1 to 2 milliseconds, demanding a prospective inrush surge of **1,600 A to 5,000 A**.

While the HiBlade's **14S3P 45Ah hybrid-solid-state pouch cells** (135Ah nominal, 50.0 V nominal / 60.2 V maximum) pass severe safety abuse tests without thermal runaway, repeatedly exposing a 3P solid-state pack to uncontrolled impulses above **400 A (> 3C)** causes cumulative micro-degradation of the solid-electrolyte interface and degrades cycle life.



To deliver plug-and-play starting of large inverter banks while guaranteeing zero cell degradation, and to be **UL / DNV certification ready**, the HiBlade integrates a coordinated **3-Tier Protection Architecture** combining an off-board high-pulse active pre-charge circuit, a 12-MOSFET solid-state primary switch, and an NXP Battery Junction Box (BJB) pyro-fuse.

Fig 1: HiBlade 14S3P stack with Quasar 12-MOSFET BMS is fixed to a heat-dissipating aluminium cage around the cells

> **Key Engineering Advantage: 100% Automatic Solid-State Commissioning**
> Installers never need to wire external pre-charge resistors, hold manual bypass push-buttons, or replace sacrificial inrush fuses. Pressing the HiBlade ON button initiates an automated pre-charge and impedance diagnostic sequence that tames a 5,000 A prospective capacitor surge into a controlled **80 A ramp** before closing the main solid-state power path.

Engineering Insights and filed patent:

Pre-charge as a load-characterisation measurement. The BMS classifies what is on the bus (capacitor bank alone, monitoring loads, inverter left awake, wiring fault) before the main switch is ever closes. The abort flag then becomes a diagnosis (“inverter on the aft bus is drawing ~4 Ω, switch it to standby”) rather than a generic OVERLOAD_ON_STARTUP. For Quasar Care: the capacitance estimate can be written to the equipment node in the semantic model and trended across start-ups for capacitor ageing.

Impedance-derived handover threshold. The HiBlade already measures its own internal resistance by EIS, and can measure the external loop resistance from the pre-charge curve. So the handover ΔV can be computed live: ΔV_max = (cell C-rate limit from the ageing reference) × (measured R_loop), tightening as the pack ages or as a connection corrodes. A window derived from measured pack and loop impedance and the per-cell-group current limit is novel and impactful.

This is the fifth of five patents filed on HiBlade and Quasar BMS.

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2. Automatic Active Pre-Charge Sequence (4-Stage State Machine)

Every time the HiBlade battery is switched on, the Quasar BMS keeps the 12 main power MOSFETs open and engages a high-pulse **0.68 Ω / 50 W chassis-mounted wire-wound pre-charge stage** thermally bonded to the battery's aluminium structural end-plate, actively monitoring load-side bus voltage (V_{bus}) in real time:

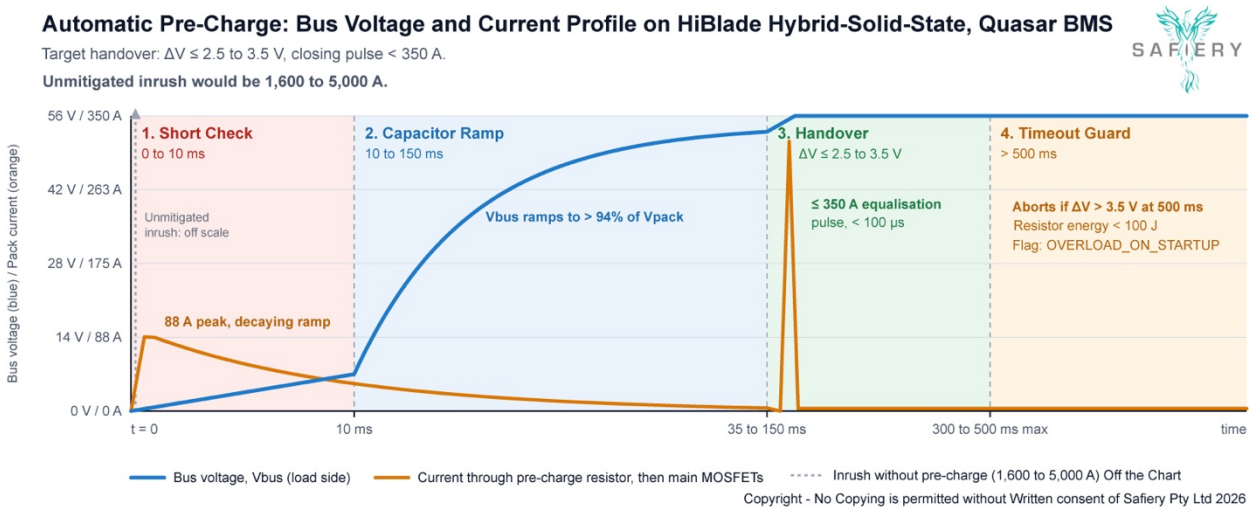


Figure 2: Automatic pre-charge bus voltage (V_{bus}) and current profile versus unmitigated inrush.

Stage 1 (0 to 10 ms): Verifies V_{bus} rises off 0 V; aborts at ≤ 88 A if a dead short exists.
Stage 2 (10 to 150 ms): Charges up to 40,000 µF capacitor banks through the pre-charge resistor.
Stage 3 (handover): Main MOSFETs close only when ΔV ≤ 2.5 V to 3.5 V, keeping the closing pulse ≤ 350 A.
Stage 4 (timeout guard): A 500 ms timeout protects the pre-charge resistor against stalled start-ups.

3. Why Main Switch Handover Requires ΔV ≤ 2.5 V to 3.5 V

When the 12 main power MOSFETs close to bypass the pre-charge resistor, any remaining voltage difference ($\Delta V = V_{pack} - V_{bus}$) discharges instantly across the total system loop resistance (R_{loop}). Because the HiBlade's 14S3P cells have an internal resistance of just **4.67 mΩ**, total system loop resistance, including busbars, current shunt, MOSFETs, cables, and capacitor ESR, is typically **~10 mΩ**.

Closing into a 10 mΩ loop with even a 7 V gap would trigger a **700 A equalisation spike** ($I = \Delta V / R_{loop}$), violating the 400 A cell limit and tripping short-circuit protection. By waiting until **ΔV ≤ 2.5 V to 3.5 V** before closing the main MOSFETs, the HiBlade guarantees the handover spike remains **≤ 350 A for < 100 µs**.

> **Commissioning Guideline: Parasitic DC Loads and Inverter Power Switches During Start-Up**
>
> During pre-charge, any active DC load forms a voltage divider with the 0.68 Ω pre-charge resistor. DC monitoring electronics (for example a Victron Cerbo GX, relays, or bilge monitors drawing **≤ 300 W / ≥ 10 Ω**) can remain powered continuously. Heavy DC loads or inverters left switched ON (whose internal supplies wake up above under-voltage lockout and draw high constant power, equivalent to **< 5 Ω**) will prevent V_{bus} from reaching the final 3 V handover window.
>
> If ΔV does not reach ≤ 3.5 V within **300 to 500 ms**, the BMS safely aborts start-up and flags `OVERLOAD_ON_STARTUP`.
>
> **Best practice:** Place main AC inverters in *OFF* or *Standby* mode before pressing the battery ON button, then switch the inverter ON once the battery is active.

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4. Coordinated Protection Matrix and Operating Specifications

The HiBlade coordinates resettable solid-state MOSFET switching with an irreversible, automotive-grade **NXP BJB pyro-fuse** so that normal field overloads and wiring shorts never sacrifice the non-serviceable pyro-fuse:

PROTECTION PARAMETER	HIBLADE 14S3P RATING	ACTIVE LAYER	SYSTEM BEHAVIOUR AND PURPOSE
Continuous discharge	**150 A to 200 A** (continuous)	**Normal operation**	Conservative continuous rating within the 3C (405 A) cell thermal window.
Overcurrent protection	**250 A to 300 A** (6 seconds)	**Primary MOSFETs**	Supports heavy inverter surge loads while staying strictly below 400 A.
Transient surge protection	**350 A** (10 ms to 30 ms)	**Primary MOSFETs**	Supports motor and compressor start transients below the 400 A cell limit.
Supported inverter inrush	**Up to 5,000 A prospective** *(up to 40,000 µF DC bus)*	**0.68 Ω active pre-charge**	Automatically clamps multi-kA capacitor surges down to an **80 A ramp**.
Main switch handover peak	**≤ 350 A peak** (< 100 µs)	**ΔV ≤ 3.5 V gate lock**	Main MOSFETs close only when V_{bus} is within 2.5 V to 3.5 V of V_{pack}.
Pre-charge guard window	**10 ms short check**, **300 to 500 ms** maximum timeout	**Off-board pre-charge**	Aborts into dead shorts at 10 ms; caps resistor energy below 100 J on stalled starts.
Short-circuit protection (SCP)	**400 A** (100 µs to 150 µs) *(100% resettable)*	**Primary MOSFETs**	Always active. Clears external faults cleanly inside the 720 A MOSFET turn-off SOA.
Ultimate catastrophic protection *(UL and DNV compliance)*	**> 720 A for > 500 µs** or **> 400 A for > 5 ms**	**Secondary pyro-fuse (NXP BJB)**	Non-serviceable backup. Fires only if fault di/dt exceeds the 720 A MOSFET turn-off SOA or if primary MOSFETs fail shorted.

5. How the 12-MOSFET Bank and NXP BJB Pyro-Fuse Coordinate

A critical requirement in high-density battery design is ensuring the solid-state BMS never attempts to open its MOSFETs outside their Safe Operating Area (SOA), while preventing nuisance trips of the sacrificial pyro-fuse:

- **Primary resettable clearing (< 720 A SOA):** The Quasar BMS uses 12 parallel back-to-back MOSFETs clamped by 88 V TVS diodes, providing a verified safe turn-off ceiling of **720 A**. By setting hardware short-circuit protection at **400 A (100 to 150 µs)**, even worst-case fault current overshoot (~600 to 650 A during turn-off) is interrupted cleanly and resettably by the MOSFETs.
- **High di/dt turn-off inhibit (> 720 A for > 500 µs):** If an ultra-low-impedance dead short occurs while the battery is already online and current climbs past **720 A** before the MOSFETs can open, the BMS keeps the MOSFETs *closed* (the 12-FET bank can safely conduct up to 21,600 A for 300 µs without thermal failure) and commands the **NXP BJB to fire the high-speed pyro-fuse**.
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Let’s Build Something together

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